REMARKS/ARGUMENTS

After entry of this amendment, claims 1-25 will remain pending in this application. Claims 12 and 16 have been amended. Support for the amended claims can be found in the specification. No new matter has been added.

Claims 1-5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Benavides, United States patent number 6,618,827. Claims 12 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Mattison, United States patent number 5,867,332. Reconsideration of these rejections and allowance of the pending claims in light of these amendments and remarks is respectfully requested.

Title

The title has been objected to. Accordingly, the title has been changed to BUILT-IN SELF-TEST CIRCUITRY FOR INTEGRATED CIRCUITS.

Abstract

The abstract has been object to and amended.

Formalities

The disclosure is objected to. Specifically, the pending office action states that a detailed description of a retiming circuit is not provided. (See pending office action, page 2 paragraph 3.) Claims 6-7, 9-10, and 13-14 are objected to for similar reasons.

Descriptions, examples, and timing diagrams of retiming circuits are provided in the specification. For example, paragraph 35 of the pending application describes the function of two retiming circuit 550 and 555 as retiming the input signal to a clock signal. Paragraph 41 of the pending application gives a flip-flop as an exemplary circuit that can be used as a retiming circuit. As another example, paragraph 49 illustrates a timing diagram of the signals at the input, clock, and output of a retiming circuit.

Since retiming circuit functions are described, example circuits are given, and their timing is shown, applicants request that this objection be withdrawn.

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Claims 16-25 are also objected to. This objection has been obviated by

amendment.

Claim 1

Claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by

Benavides. But Benavides does not teach each and every element of this claim. For example,

claim 1 recites "<u>comparing the test output data with the delayed test output data</u> to generate a

first compare signal." Benavides does not provide this feature.

The pending office action cites Figure 1 of Benavides as teaching this limitation.

(See pending office action, page 3, paragraph 6.) But Benavides does not teach a comparator

that compares test output data with delayed test output data as required.

Rather, Figure 1 of Benavides shows a single comparator 400 that is connected to

compare the output of the delay adjustment circuit 200 with the output of the comparison control

circuit 300. There is no comparator that is connected to compare selected test data at the input of

the delay adjustment circuit 200 with the output of the delay adjustment circuit 200.

Accordingly , Benavides does not teach <u>comparing the test output data with the delayed test</u>

<u>output data</u> as required by the claim.

For at least this reason, claim 1 should be allowed.

Claim 12

Claim 12 stands rejected under 35 U.S.C. 102(b) as being anticipated by Mattison.

But Mattison does not teach each and every element of this claim. For example, claim 12, as

amended, recites "<u>a plurality of logic elements coupled to receive a test data input</u> " Mattison

does not provide this feature.

The pending office action cites Figure 7A of Mattison as teaching each and every

limitation of this claim. (See pending office action, page 4, paragraph 8.) But Mattison does not

provide a plurality of logic elements coupled to receive a test data input as required by the claim.

Rather, Mattison teaches a data decoder or separator for use in disk drive

applications. (See Mattison, abstract and background.) The data input to the circuit shown is

data read magnetically read from a hard drive. (See Mattison, background.) Accordingly, the

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data is not test data as required by the claim. Moreover, Mattison does not show a plurality of logic elements as required.

Also, claim 12, as amended, recites "<u>wherein the control signal is based on the test data input</u>." Mattison does not provide this feature.

The pending office action cites the signal at the output of gate 118 in Figure 7A of Mattison as teaching the required control signal. (See pending office action, page 5, line 3.) But this signal is labeled as an encoded data signal. Figure 7A shows that this signal is the exclusive-OR of the delayed data signal from the disk drive and the output of the PLL 112. As such, this is a modified version of the data read from the disk drive. It is not a control signal <u>based on the test data input</u> as required.

For at least these reasons, claim 12 should be allowed.

Other claims

The other claims depend on the above claims and should be allowed for at least the same reasons and for the additional limitations they recite.
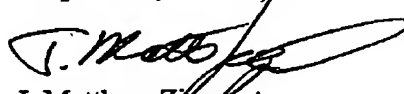
CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

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If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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